PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Branko Kovacevic et al.

For:	METHOD AND SYSTEM FOR HANDLING DATA		
App. No.:	09/491,121	Filed:	January 24, 2000
Examiner:	Shawn S. An	Group Art Unit:	2613
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The Board of Patent Appeal and Interferences
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

BRIEF ON APPEAL

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This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(1)):

TABLE OF CONTENTS

The final page of this brief before the beginning of the Appendix of Claims bears the agent's signature.

REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is ATI Technologies, Inc.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

There are no interferences or other appeals that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS (37 C.F.R. § 41.37(c)(1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

There are thirty-five (35) claims pending in the application (claims 1-35).

B. STATUS OF ALL THE CLAIMS

1. Claims pending:

   Claims 1-35.

2. Claims withdrawn from consideration but not canceled:

   3-5, 11, 12, 25-32 and 35.

3. Claims allowed:

   NONE.

4. Claims objected to:

   NONE.

5. Claims rejected:

   Claims 1, 2, 6-10, 13-15, 20-24, 33 and 34 are rejected under 35 U.S.C. § 102(b).

   Claims 16-19 are rejected under 35 U.S.C. § 103(a).

6. Claims canceled:

NONE.

C. CLAIMS ON APPEAL

There are seventeen (19) claims on appeal, claims 1, 2, 6-10 and 13-24.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

No amendments have been submitted subsequent to the Final Rejection.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

The following summary is provided to give the Board the ability to quickly determine where the claimed subject matter appealed herein is described in the present application and is not to limit the scope of the claimed invention.

Independent claim 1 recites the limitations of a system for processing transport stream data, the system comprising a framer module and a first parser module. The frame module has an input node to receive the transport stream data, a data output node to provide a frame data which is a representation of the transport stream data, and a data enable output node to provide a signal to indicate a valid data on the data output node. The first parser module has a data input node coupled to the data output of the framer module to receive the framer data, a data enable input node coupled to data the data enable output node of the framer module, a data output node to provide a first parser data when the framer data is a first data type, wherein the first parser data is a representation of the framer data, a first data enable output node to provide a signal to indicate a valid first parser data on the data output node of the first parser, and a second data enable output node to provide a signal to indicate the framer data is of a second data type.

Independent claim 13 recites the limitations of a system for processing transport stream data, the system comprising a framer having a modular layout and a first parser having a modular layout separate from the modular layout of the framer. The framer comprises an input node to receive the transport stream data, a data output node to provide a framer data based upon the transport stream data, and a data enable output node to provide a signal to indicate a valid data

on the data output node. The first parser comprises a data input node coupled to the data output node of the framer to receive the framer data, a first data enable output node to provide a signal to indicate a first type of framer data, and a second data enable output node to provide a signal to indicate a second type of framer data.

Independent claim 16 recites the limitations of a method of parsing a data packet, the method comprising: providing a start indicator to a first parser, the start indicator indicating a first data block of the data packet, the data packet having a predetermined number of data blocks; analyzing at the first parser at least a portion of the first N data blocks after the start of the data packet to determine a data type of a subsequent data block of the data packet, wherein the subsequent data block is after the first N data blocks; enabling a second parser to receive the subsequent data block when the data type of the subsequent data block is a first data type; and enabling a third parser to receive the subsequent data block when the data type of the subsequent data block is a second data type.

Independent claim 22 recites the limitations of a system for storing packetized data, the system comprising: a means for receiving a transmitted data packet, a first parser means for analyzing a header of the data packet before a payload header is received, and a second parser means physically separate from the first parser means for analyzing the payload header.

Figures 5 and 7 (reproduced below) of the Present Application and their corresponding disclosure are illustrative of exemplary embodiments of the subject matter of claims 1, 13, 16 and 22.

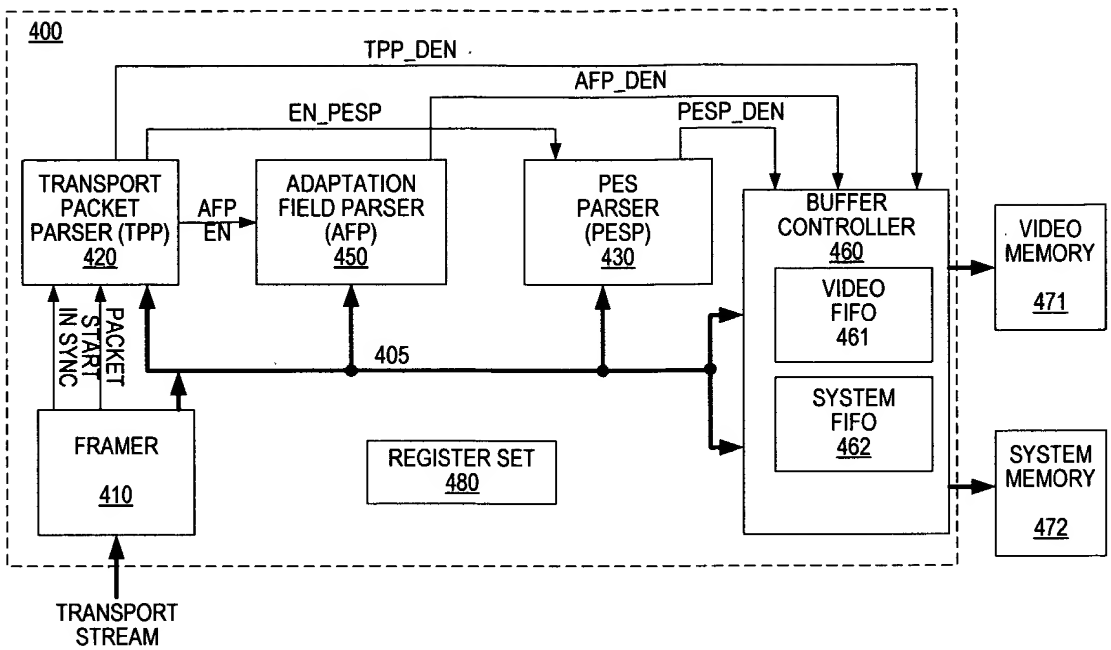


FIG. 5

The Present Application, Figure 5

Figure 5 illustrates a transport stream core 400 comprising a framer 410 and a plurality of parsers including a transport packet parser (TPP) 420, a PES parser (PESP) 430, and an adaptation field parser (AFP) 450. As disclosed by the Present Application, the framer 410 receives at an input node a raw transport stream (labeled "TRANSPORT STREAM") that is "analyzed to isolate and provide individual transport stream packets (TSP) to the bus 405" where the bus 405 (e.g, a data output node), in one embodiment, receives byte wide data and "a control signal [e.g., a data enable output node] to indicate when the current byte of data is valid." See Present Application, p. 12. The framer 410 provides a signal PACKET START to indicate the first byte of a packet and a signal IN SYNC to indicate when the data on the bus 405 is synchronized by the framer 410. See Id.

As further disclosed by the Present Application, the TPP 420 is connected to the bus 405 and receives the IN SYNC and PACKET START signals, whereby parsing of a transport stream packet received via the bus 405 by the TPP 420 is enabled when the IN SYNC signal and the PACKET START signals are asserted indicating the beginning of a new packed. During parsing of the header portion of a packet the PID number is obtained. Based upon the value of the PID

number, registers are updated, and a determination is made whether the TSP is to be saved, further processed, or discarded. See Id.

When the transport packet is to be saved, the TPP 420 asserts the signal TPP_DEN, which is received by the Buffer Controller 460. Based upon this enable signal, the Buffer controller 460 retrieves the packet data and stores it in a predefined memory location. Alternatively, when the transport packet is to be further processed by one of the other parsers 450 or 430, the TPP 420 asserts one of their respective enable signals (e.g., PESP_EN or AFP_EN). In response to the asserting of one of the enable signals, the respective parser further processes the packet data. As with the TPP 420, the AFP 450 and PESP 430 can assert the signals AFP_DEN or PESP_DEN, respectively, when providing packet data via the bus 405. In response to the asserted signal AFP_DEN or PESP_DEN, the buffer controller 460 receives the packet data and stores it in a predefined location. See Id.

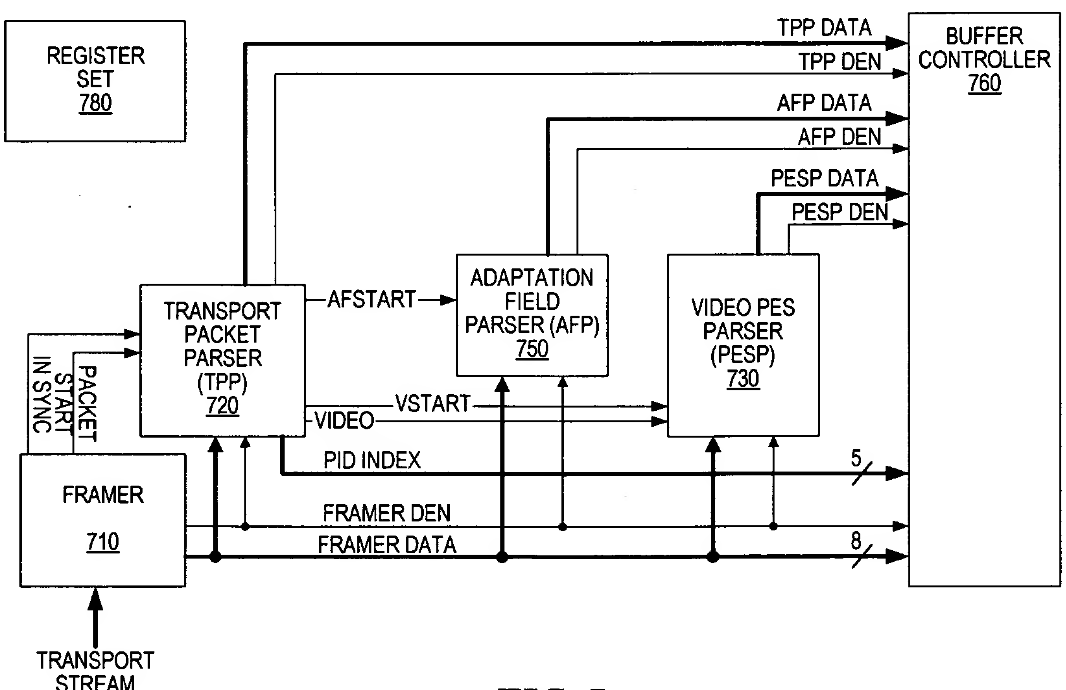


FIG. 7

The Present Application, Figure 7

Figure 7 illustrates another exemplary embodiment of a transport stream core comprising a framer 710 and a plurality of parsers, including TPP 720, AFP 750 and PESP 730. The framer 710 provides transport stream data (FRAMER DATA) and an enable signal FRAMER DEN to

the parsers 720, 730 and 750. See Present Application, p. 13. As disclosed by the Present Application, "[t]he FRAMER DATA is qualified by the signal FRAMER DEN, which is an enable signal. The signal FRAMER DEN is asserted during each valid FRAMER DATA." Id. As with the transport stream core of Figure 5, the parsers 720, 730 and 750 may obtain the FRAMER DATA based on the signal FRAMER DEN, parse the applicable portion of the FRAMER data, and provide the parsed data (TPP DATA, AFP DATA, and PESP DATA, respectively) to a buffer controller 760, along with enable signals TPP DEN, AFP DEN and PESP DEN, respectively, to indicate valid data. See Id.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

A. Claims 1, 2, 6-10, 13-15, 20 and 21 are rejected under 35 U.S.C. § 102(b) in view of United States Patent No. 5,559,999 to *Maturi et al* (hereinafter, "the *Maturi* reference") as set forth in the Non-Final Office Action dated April 9, 2004 (hereinafter, "the Non-Final Action") and the Final Office Action dated November 30, 2004 (hereinafter, "the Final Action").

B. Claims 22-24 are rejected under 35 U.S.C. § 102(b) in view of United States Patent No. 5,517,250 to *Hoogenboom et al* (hereinafter, "the *Hoogenboom* reference") as set forth in the Non-Final Action and the Final Action.

C. Claims 16-19 are rejected under 35 U.S.C. § 103(a) over the *Hoogenboom* reference in view of United States Patent No. 6,043,828 to *Ort* (hereinafter, "the *Ort* reference") as set forth in the Non-Final Action and the Final Action.

VII. ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

Based on the arguments and issues below, none of the claims stand or fall together, because in addition to having different scopes, each of the independent claims has a unique set of issues relating to its rejection and appeal as indicated in the arguments below.

A. Rejection of Claims 1, 2, 6-10, 13-15, 20 and 21 under 35 U.S.C. § 102(b):

At page 2 of the Final Action, claims 1, 2, 6-10, 13-15 and 20-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by the *Maturi* reference.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id.

The Final Action asserts that the *Maturi* reference discloses all of the limitations recited by claims 1, 2, 6-10, 13-15, 20 and 21. Contrary to the assertions of the Final Action, the *Maturi* reference fails to disclose each and every limitation recited by claims 1, 2, 6-10, 13-15, 20 and 21 for at least the reasons provided below.

1) The § 102(b) Rejection of Claims 1, 2, and 6-10

Independent claim 1, from which claims 2 and 6-10 depend, is reproduced below for ease of reference:

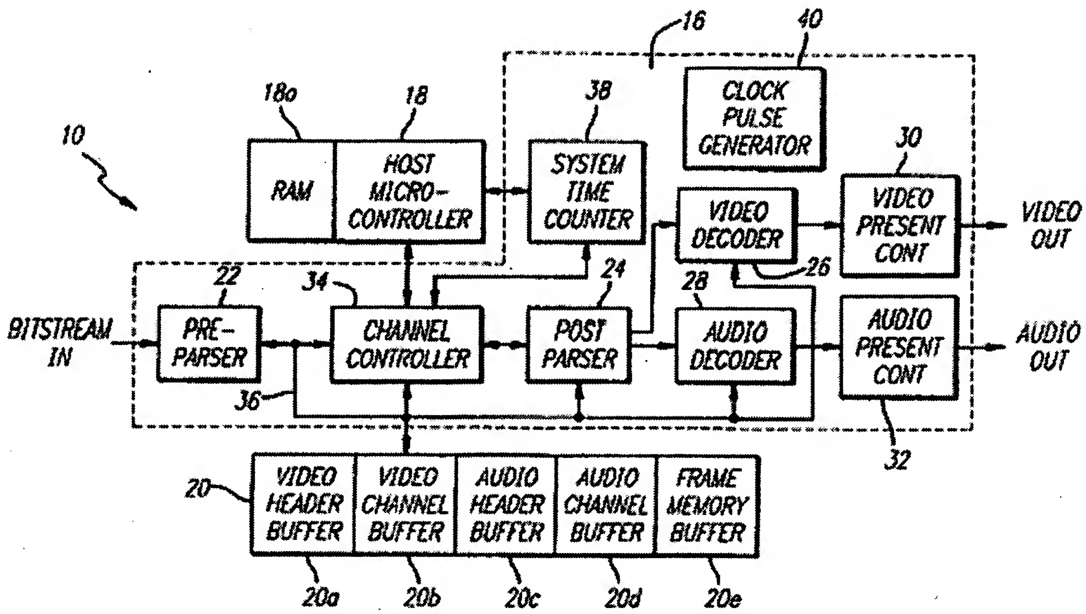
1. (Original) A system for processing transport stream data, the system comprising:

a framer module having
an input node to receive the transport stream data,
a data output node to provide a framer data which is a representation of the transport stream data, and
a data enable output node to provide a signal to indicate a valid data on the data output node;

a first parser module having
a data input node coupled to the data output of the framer module to receive the framer data,
a data enable input node coupled to data the data enable output node of the framer module;
a data output node to provide a first parser data when the framer data is a first data type, wherein the first parser data is a representation of the framer data,
a first data enable output node to provide a signal to indicate a valid first parser data on the data output node of the first parser, and
a second data enable output node to provide a signal to indicate the framer data is of a second data type.

a) The *Maturi* Reference Fails to Disclose a Framer Module Having a Data Enable Output Node as Recited By Claim 1

Claim 1 recites the limitations of a framer module having a data output node to provide a framer data which is a representation of the transport stream data and a data enable output node to provide a signal to indicate a valid data on the data output node. With respect to the data enable output node limitations, the Final Action asserts that the *Maturi* reference "clearly discloses the output of element 22 being a framer data based on transport stream data (col. 5, lines 20-36), or the output of element 22 or element 36 being a data enable output node to provide signals such as video, audio, and parsing information to indicate a valid data (inherency, also emphasized) on the data output node (22) as clearly shown in Fig. 3 [of the *Maturi* reference], nodes, arrows." Final Action, p. 3. For ease of reference, Figure 3 of the *Maturi* reference is reproduced below:



The Maturi Reference, Figure 3

Figure 3 of the *Maturi* reference illustrates that the pre-parser 22 includes an input to receive "BITSTREAM IN," and an output connected to bus 36, which the Final Action appears to consider equivalent to the data output node of the framer of claim 1. The bus 36, in turn, is connected to channel controller 34, DRAM 20, post-parser 24, audio decoder 28 and video decoder 26. Even if it is assumed, *arguendo*, that the bus 36 is equivalent to the data output node of the framer as recited by claim 1, Figure 3 of the *Maturi* reference provides no indication that either of the pre-parser 22 or the bus 36 has a data enable output node to provide a signal to indicate a valid data on bus 36 as recited by claim 1. Turning to the disclosure associated with the pre-parser 22, the *Maturi* reference teaches that:

> [t]he pre-parser 22 parses the input bitstream and captures any SCR (MPEG 1) or PCR (MPEG 2) time stamps that are included in any of the layers of the stream. The pre-parser 22, under control of the channel controller 34, causes PES video headers to be stored in the video header buffer and PES audio headers to be stored in the audio header buffer 20c.
>
> The pre-parser 22 causes PES streams of video data (access) units to be stored in the video channel buffer 20b and audio data (access) units to be stored in the audio channel buffer 20d in a First-In-First-Out (FIFO) arrangement. The starting address of each access unit stored in the buffer 20b or 20d is the address following the last address of the previous access unit.
>
> . . .

> As the pre-parser 22 begins to store a video header or an audio header in the header buffer 20a or 20c respectively, it generates a first interrupt to the microcontroller 18. The pre-parser 22 then stores the access unit following the header in the appropriate channel buffer 20b or 20d. The pre-parser 22 also captures the starting address (write pointer) of the access unit in the channel buffer 20b or 20d, and appends this starting address as a "tag" to the header stored in the header buffer 20a or 20c.
>
> As illustrated in the flowchart of FIG. 6, the host microcontroller 18 receives the first interrupt from the pre-parser 22, and extracts the presentation time stamp from the PES header stored in the header buffer 20a or 20c, together with the associated tag. The host microcontroller 18 stores these two items as an "entry" in a list in the RAM 18a. The entries in the RAM 18a provide a link between the presentation time stamps stored in the header buffer 20a or 20c and the starting addresses of the associated access units stored in the channel buffer 20b or 20d.

<u>The Maturi Reference</u>, col. 5, line 50 – col. 6, line 19.

As the above-cited passage illustrates, the *Maturi* reference discloses that the preparser 22 provides an interrupt to the microcontroller 18 to inform the microcontroller 18 that PES data has been stored in one or more of the buffers 20a-20e of the DRAM 20. In response to the interrupt, the microcontroller 18 may access the appropriate buffer of the DRAM 20 to obtain presentation time stamps and their associated tags for storage as entries in a list in the RAM 18a. Thus, while the above-cited passage teaches that the pre-parser 22 may provide an interrupt to signal that PES data has been stored in the buffers of the DRAM 20, neither the above-cited passage nor any other passage of the *Maturi* reference discloses that the pre-parser 22 (or any other element of the *Maturi* reference) provides a signal that indicates the validity of data output from the parser 22 to the bus 36. Thus, the *Maturi* reference fails to disclose the limitations of a framer module having a data enable output to provide a signal to indicate a valid data on a data output node of the framer module as recited by claim 1.

During a telephonic interview conducted on January 26, 2005 (hereinafter, "the Telephonic Interview") between the Examiner and the Appellants' representative, the Examiner conceded that the *Maturi* reference does not explicitly disclose a data enabled output node as recited by claim 1, but reaffirmed the assertion that these limitations are inherent to the disclosure of the *Maturi* reference.

Referring to the use of the inherent disclosure of a prior art reference, the M.P.E.P. provides that:

> **The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.** *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "**To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference**, and that it would be so recognized by persons of ordinary skill. **Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.**' " *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted) (The claims were drawn to a disposable diaper having three fastening elements. The reference disclosed two fastening elements that could perform the same function as the three fastening elements in the claims. The court construed the claims to require three separate elements and held that the reference did not disclose a separate third fastening element, either expressly or inherently.).
>
> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic <u>necessarily</u> flows from the teachings of the applied prior art." *Ex parte Levy,* 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original) (Applicant's invention was directed to a biaxially oriented, flexible dilation catheter balloon (a tube which expands upon inflation) used, for example, in clearing the blood vessels of heart patients). The examiner applied a U.S. patent to Schjeldahl which disclosed injection molding a tubular preform and then injecting air into the preform to expand it against a mold (blow molding). The reference did not directly state that the end product balloon was biaxially oriented. It did disclose that the balloon was "formed from a thin flexible inelastic, high tensile strength, biaxially oriented synthetic plastic material." *Id.* at 1462 (emphasis in original). The examiner argued that Schjeldahl's balloon was inherently biaxially oriented. The Board reversed on the basis that the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.).

<u>M.P.E.P.</u> § 2112 (emphasis added).

Neither the Non-Final Action nor the Final Action provide any basis for the general assertion that the data enable output node limitations of claim 1 are inherent to the disclosure of the *Maturi* reference. Thus, the Final Action fails to establish that the data enable output node limitations are "necessarily present" or "necessarily flow" from the teachings of the *Maturi*

reference as is required to establish their inherency. See In re Robertson; see also Ex parte Levy (supra). Moreover, an attempt to establish these limitations are inherent to the teachings of the *Maturi* reference would fail as such a data enable output node would not be necessarily present in the system disclosed by the *Maturi* reference. One of ordinary skill in the art will appreciate that there are numerous known techniques for signaling that data is on a bus, including, for example, utilizing a predefined sequence (e.g., a training sequence) at the start of a header of a packet that encapsulates the data, transmitting data on the bus only at certain predefined time periods or in alignment with certain clock pulses, and the like. As one of ordinary skill in the art could identify numerous techniques for indicating the validity of data on a bus, the use of a data enable output mode to provide a signal indicating such validity is only one possible technique and therefore is not inherent to the system of the *Maturi* reference.

As established above, the *Maturi* reference fails to disclose, either explicitly or implicitly, the limitations of a data enable output node to provide a signal to indicate a valid data on a data output node. Accordingly, the Final Action fails to establish that the *Maturi* reference discloses a framer module having a data enable output node as recited by claim 1.

b) The *Maturi* Reference Fails to Disclose a First Parser Module Having a Data Enable Input Node as Recited by Claim 1

Claim 1 further recites the limitations of a first parser module having a data enable input node coupled to the data enable output node of the framer module. As noted above in section (a), the *Maturi* reference fails to disclose a framer module having a first data enable output node, so the *Maturi* reference necessarily fails to disclose a first parser having a data enable input node coupled to the data enable output node of a framer module.

c) The *Maturi* Reference Fails to Disclose a First Parser Module Having a First and Second Data Enable Output Nodes as Recited by Claim 1

Claim 1 further recites the limitations of the first parser module having a first data enable output node to provide a signal to indicate a first type of framer data and a second data enable output node to provide a second type of framer data. With reference to these limitations, the Final Action asserts that the *Maturi* reference "clearly discloses enable output nodes (outputs [of]

20, 24) for providing signals to indicate first (frame memory data, 20e) or second type of framer data (video data to 26) respectively, as recited in claims 1 and 13." Final Action, p. 3. As depicted by Figure 3 of the *Maturi* reference (reproduced above), elements 20 and 24 represent a DRAM 20 and a post-parser 24, respectively. Based on the above-cited passage of the Final Action, it appears that the Final Action considers that the combination of the DRAM 20 and the post-parser 24 as equivalent to the first parser module recited by claim 1. The sole reference to the post-parser 24 in the corresponding passages of the *Maturi* reference discloses only that "[t]he post-parser 24, under control of the channel controller 34, causes video and audio access units to be read out of the DRAM 20 and applied to the appropriate decoder 26 or 28." The Maturi Reference, col. 7, lines 6-9. This passage does not disclose that the post-parser 24 has any type of output to provide a signal indicating a type of data output by the post-parser 24, so the *Maturi* reference necessarily fails to disclose that the post-parser comprises a data enable output node to provide a type of framer data as recited by claim 1. Similarly, the *Maturi* reference fails to disclose that the DRAM 20 has a data enable output node to provide a type of framer data as recited by claim 1. For at least these reasons, the *Maturi* reference fails to disclose the limitations of a first parser module having a first data enable output node to provide a signal to indicate a first type of framer data and a second data enable output node to provide a second type of framer data as recited by claim 1.

d) The *Maturi* Reference Fails to Anticipate Claims 1, 2, and 6-10

As noted above, the *Maturi* reference fails to disclose the limitations of claim 1 of: a framer module having a data enable output node to provide a signal indicating a valid data; a first parsing module having a data enable input node coupled to a data enable output node of a framer module; and a first parser module having a first data enable output node to provide a signal to indicate a first type of framer data and a second data enable output node to provide a second type of framer data. Thus, the *Maturi* reference fails to disclose each and every limitation of claim 1, as well as claims 2 and 6-10 at least by virtue of their dependency on claim 1. Accordingly, the Final Action fails to establish that the *Maturi* reference anticipates claims 1, 2 and 6-10 under 35 U.S.C. § 102(b). Claims 1, 2 and 6-10 therefore should be allowable under 35 U.S.C. § 102(b).

2) The § 102(b) Rejection of Claims 13-15, 20 and 21

Independent claim 13, from which claims 14, 15, 20 and 21 depend, is reproduced below for ease of reference:

13. (Original) A system for processing transport stream data, the system comprising:

a framer having a modular layout, the framer comprising
an input node to receive the transport stream data,
a data output node to provide a framer data based upon the transport stream data, and
a data enable output node to provide a signal to indicate a valid data on the data output node;
a first parser having a modular layout separate from the modular layout of the framer, the first parser comprising:
a data input node coupled to the data output node of the framer to receive the framer data,
a first data enable output node to provide a signal to indicate a first type of framer data,
a second data enable output node to provide a signal to indicate a second type of framer data.

a) The *Maturi* Reference Fails to Disclose a Framer Having a Data Enable Output Node as Recited By Claim 13

Claim 13 recites the limitations of a framer having a data output node to provide a framer data which is a representation of the transport stream data and a data enable output node to provide a signal to indicate a valid data on the data output node. As established above with reference to claim 1, the *Maturi* reference fails to disclose, either explicitly or inherently, the limitations of a data enable output node to provide a signal to indicate a valid data on a data output node. Accordingly, the Final Action fails to establish that the *Maturi* reference discloses a framer having a data enable output node as recited by claim 13.

b) The *Maturi* Reference Fails to Disclose a First Parser Having a Data Enable Input Node as Recited by Claim 13

Claim 13 further recites the limitations of a first parser having a data enable input node coupled to the data enable output node of the framer. As established above with reference to claim 1, the *Maturi* reference fails to disclose a framer having a first data enable output node, so the *Maturi* reference necessarily fails to disclose a first parser having a data enable input node coupled to the data enable output node of a framer as recited by claim 13.

c) The *Maturi* Reference Fails to Disclose a First Parser Having a First and Second Data Enable Output Nodes as Recited by Claim 13

Claim 13 further recites the limitations of the first parser having a first data enable output node to provide a signal to indicate a first type of framer data and a second data enable output node to provide a second type of framer data. As established above with reference to claim 1, the *Maturi* reference fails to disclose the limitations of a first parser having a first data enable output node to provide a signal to indicate a first type of framer data and a second data enable output node to provide a second type of framer data as recited by claim 13.

d) The *Maturi* Reference Fails to Disclose a First Parser Having a Modular Layout Separate From a Modular Layout of a Framer as Recited by Claim 13

Claim 13 further recites the limitations of a first parser having a modular layout separate from a modular layout of a framer. Neither the Non-Final Action nor the Final Action addresses these limitations in any specific manner. The Final Action therefore fails to establish a *prima facie* case of anticipation of these limitations. Moreover, the *Maturi* reference fails to disclose these limitations.

e) The *Maturi* Reference Fails to Anticipate Claims 13-15, 20 and 21

As noted above, the *Maturi* reference fails to disclose the limitations of claim 13 of: a framer having a data enable output node to provide a signal indicating a valid data; a first parsing module having a data enable input node coupled to a data enable output node of a framer; a first parser having a first data enable output node to provide a signal to indicate a first type of framer data and a second data enable output node to provide a second type of framer data; and a first parser having a modular layout separate from a modular layout of a framer. Thus, the *Maturi* reference fails to disclose each and every limitation of claim 13, as well as claims 14, 15, 20 and 21 at least by virtue of their dependency on claim 13. Accordingly, the Final Action fails to establish that the *Maturi* reference anticipates claims 13-15, 20 and 21 under 35 U.S.C. § 102(b). Claims 13-15, 20 and 21 therefore should be allowable under 35 U.S.C. § 102(b).

B. Rejection of Claims 22-24 under 35 U.S.C. § 102(b):

At page 2 of the Final Action, claims 22-24 were rejected under 35 U.S.C. § 102(b) as being anticipated by the *Hoogenboom* reference. The Final Action asserts that the *Hoogenboom* reference discloses all of the limitations recited by claims 22-24. Contrary to the assertions of the Final Action, the *Hoogenboom* reference fails to disclose each and every limitation recited by claims 22-24 for at least the reasons provided below.

Independent claim 22, from which claims 23 and 24 depend, is reproduced below for ease of reference:

> 22. (Original) A system for storing packetized data, the system comprising:
>
> a means for receiving a transmitted data packet;
> a first parser means for analyzing a header of the data packet before a payload header is received; and
> a second parser means physically separate from the first parser means for analyzing the payload header.

a) The *Hoogenboom* Reference Fails to Disclose A First Parser Means for Analyzing a Header of a Data Packet Before a Payload Header is Received as Recited By Claim 22

Claim 22 recites the limitations of a first parser means for analyzing a header of a data packet before a payload header is received. With respect to these limitations, the Final Office Action asserts that the *Hoogenboom* reference "clearly discloses a transport parser means 32 for analyzing a header of the data packet (Fig. 3, 82) before a payload header is received (inherently receives transmitted packet header before the payload so as to properly parse the transport packets)(col. 6, lines 23-28) as recited in claim 22." Final Action, p. 3. For ease of reference, Figure 3 of the *Hoogenboom* reference and the cited passage of the *Hoogenboom* reference are reproduced below:

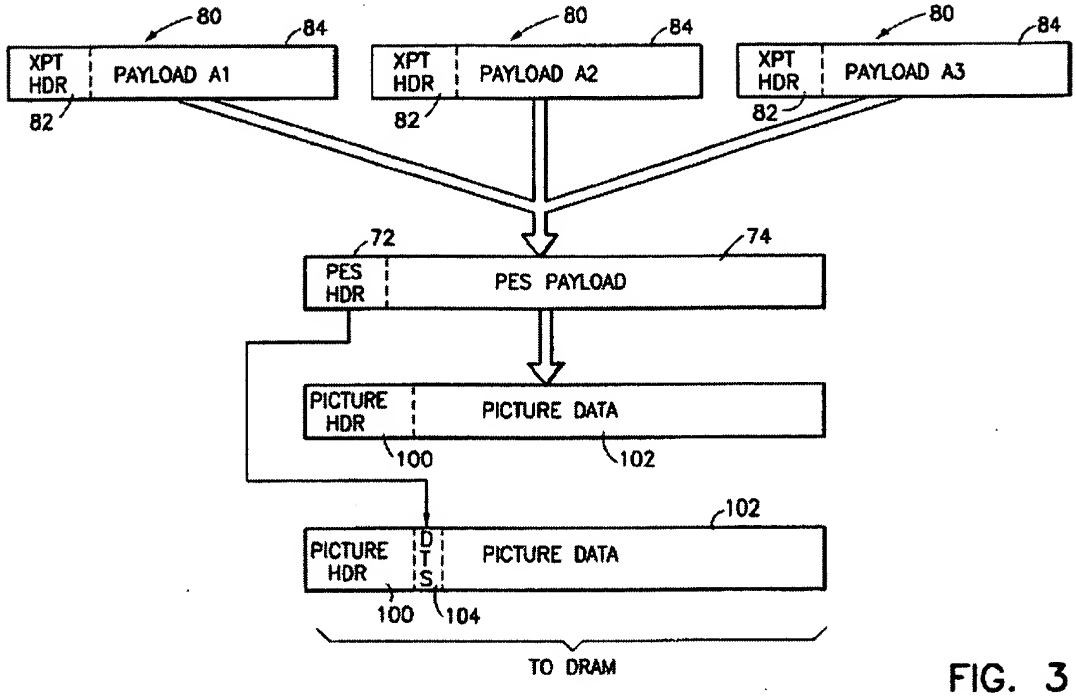


FIG. 3

The Hoogenboom Reference, Figure 3

> The video decompression processor 20 receives a clock signal via terminal 12. The clock provides timing information that is used, e.g., to enable a transport syntax parser 32 to recover timing information and video information from transport packets contained in a packetized data stream input via terminal 10. An acquisition and error management circuit 34 utilizes a program clock reference (PCR) and decode time stamp (DTS) detected by a video syntax parser 40 to synchronize the start of picture decoding. This circuit sets vertical synchronization and provides global synchronization for all video decode and display functions.

The Hoogenboom Reference, col. 6, lines 23-33.

Neither Figure 3 of the *Hoogenboom* reference nor the above-cited passage of the *Hoogenboom* reference provide any disclosure related to analyzing a header of a data packet before a payload header is received as recited by claim 22. The sole passage of *Hoogenboom* related to the functionality of element 32 states only that "[a] plurality of transport packets 80 are received by the transport syntax parser 32, which strips the payload information that is necessary from successive transport packets to reconstruct a PES payload 74." The Hoogenboom Reference, col. 9, lines 25-27. This passage fails to mention a header at all, so it necessarily fails to disclose analyzing a header, much less analyzing a header of a data packet before a payload

header is received as recited by claim 22. Moreover, no other passage of *Hoogenboom* provides any such disclosure. While the Final Action asserts that the element 32 "inherently receives transmitted packet header before the payload so as to properly parse the transport packets," this subject matter is not recited by claim 22. Claim 22 recites the limitations of "**analyzing** a header of a data packet before a payload header is received," not "**receiving** a packet header before the payload" as the Final Action provides. Further, one of ordinary skill in the art will appreciate that a transport packet conventionally is received in its entirety (e.g., so that a cyclical redundancy check may be performed) and buffered before the transport packet is parsed. Thus, the Final Action fails to establish that the *Hoogenboom* reference explicitly or inherently discloses the limitations of claim 22 of a transport parser means for analyzing a header of a data packet before a payload header is received.

b) The *Hoogenboom* Reference Fails to Disclose A Second Parser Physically Separate from the First Parser Means as Recited by Claim 22

Claim 22 further recites the limitations of a second parser means physically separate from the first parser means. With respect to these limitations, the Final Action asserts that the *Hoogenboom* reference "clearly discloses the elements 32 and 40 being physically separate in a processor (20)." Final Action, p. 3. However, the Final Action fails to cite any passage of the *Hoogenboom* reference that "clearly discloses" these limitations. Contrary to the assertions of the Final Action, the *Hoogenboom* reference fails to disclose that elements 32 and 40 are physically separate. Although illustrated as separate features in Figure 1, it will be appreciated that the *Hoogenboom* reference characterizes Figure 1 as a "block diagram of a video decompression monitor ..." and thus illustrates the functional, but not physical, layout of the video decompression monitor. The Hoogenboom Reference, col. 5, lines 43-45. Accordingly, the Final Action fails to establish that the *Hoogenboom* reference discloses the limitations of a second parser means physically separate from the first parser means as recited by claim 22.

c) The *Hoogenboom* Reference Fails to Anticipate Claims 22-24

As noted above, the *Hoogenboom* reference fails to disclose the limitations of claim 22 of: a first parser means for analyzing a header of a data packet before a payload header is received; and a second parser means physically separate from the first parser means. Thus, the

Hoogenboom reference fails to disclose each and every limitation of claim 22, as well as claims 23 and 24 at least by virtue of their dependency on claim 22. Accordingly, the Final Action fails to establish that the *Hoogenboom* reference anticipates claims 22-24. Claims 22-24 therefore should be allowable under 35 U.S.C. § 102(b).

C. Rejection of Claims 16-19 under 35 U.S.C. § 103(a):

At page 5 of the Final Action, claims 16-19 were rejected under 35 U.S.C. § 103(a) as unpatentable over the *Hoogenboom* reference in view of the *Ort* reference. According to 35 U.S.C. § 103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art of such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing *a prima facie* case of obviousness. In re Fritch, 972 F.2d 1260,1262,23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, *9* F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce *a prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of

ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. Id.

The Final Action asserts that the proposed combination of the *Hoogenboom* and *Ort* references discloses or suggests the limitations of claims 16-19. In contrast with the assertions of the Final Action, neither the *Hoogenboom* reference nor the *Ort* reference discloses or suggests, alone or in combination, each and every limitation of claims 16-19.

Independent claim 16, from which claims 17-19 depend, is reproduced below for ease of reference:

> 16. (Previously Presented) A method of parsing a data packet, the method comprising:
> providing a start indicator to a first parser, the start indicator indicating a first data block of the data packet, the data packet having a predetermined number of data blocks;
> analyzing at the first parser at least a portion of the first N data blocks after the start of the data packet to determine a data type of a subsequent data block of the data packet, wherein the subsequent data block is after the first N data blocks;
> enabling a second parser to receive the subsequent data block when the data type of the subsequent data block is a first data type; and
> enabling a third parser to receive the subsequent data block when the data type of the subsequent data block is a second data type.

a) The *Hoogenboom* and *Ort* References Fail to Disclose or Suggest Analyzing at Least a Portion of A First N Data Blocks of a Data Packet to Determine a Data Type of a Subsequent Data Block of the Data Packet as Recited By Claim 26

Claim 16 recites the limitations of analyzing at a first parser at least a portion of a first N data blocks after the start of a data packet to determine a data type of a subsequent data block of the data packet, wherein the subsequent data block is after the first N data blocks. With respect to these limitations, the Final Action asserts that the *Hoogenboom* reference "clearly discloses . . . analyzing at least a portion of the first N data blocks (video information, or pictures comprising macroblocks, which comprises [sic] blocks)(col. 6, lines 23-28; col. 11, lines 11-18)." Final Action, p. 4. The Non-Final Action makes reference to element 102 of Figure 3 of the *Hoogenboom* reference. Non-Final Action, p. 6. Neither the Non-Final Action nor the Final

Action rely or otherwise mention the *Ort* reference with regard to these limitations. For ease of reference, the cited passages of the *Hoogenboom* reference are reproduced below (Figure 3 of the *Hoogenboom* reference is reproduced above):

> The video decompression processor 20 receives a clock signal via terminal 12. The clock provides timing information that is used, e.g., to enable a transport syntax parser 32 to recover timing information and video information from transport packets contained in a packetized data stream input via terminal 10. An acquisition and error management circuit 34 utilizes a program clock reference (PCR) and decode time stamp (DTS) detected by a video syntax parser 40 to synchronize the start of picture decoding. This circuit sets vertical synchronization and provides global synchronization for all video decode and display functions.

The Hoogenboom Reference, col. 6, lines 23-28.

> The transport syntax parser 32 will detect the presence of complete pictures in the FIFO portion of DRAM 22 by monitoring the occurrence of picture start codes and sequence end codes. If the decoder, upon examining the number of pictures in the FIFO, determines that at the start of decode time there is not an entire picture in the FIFO, then it is assumed that a skipped picture has occurred at the encoder.

Id., col. 11, lines 11-18.

Neither Figure 3 nor the above-cited passages of the *Hoogenboom* reference disclose or suggest the analysis of the first set of data blocks following the start of a data packet. Likewise, they fail to disclose or suggest that any set of blocks is analyzed to determine the data type of a subsequent data block. Moreover, they fail to disclose or suggest that any such analysis is performed by a first parser. Accordingly, the cited passages of the *Hoogenboom* reference necessarily fail to disclose or suggest the limitations of analyzing at a first parser at least a portion of a first N data blocks after the start of a data packet to determine a data type of a subsequent data block of the data packet, wherein the subsequent data block is after the first N data blocks as recited by claim 16. Instead, the passage at col. 6, lines 23-28 discloses the use of a clock signal for timing information purposes and the passage at col. 6, lines 23-28 of the *Hoogenboom* reference merely discloses that the transport syntax parser 32 detects complete pictures in the DRAM 22 "by monitoring the occurrence of picture start codes and sequence end codes." Accordingly, as the Final Action fails to establish that the *Hoogenboom* reference discloses or suggest the limitations of analyzing at a first parser at least a portion of a first N data blocks after the start of a data packet to determine a data type of a subsequent data block of the

data packet as recited by claim 16 and as the Final Action makes no assertion that these limitations are discloses or suggested by the *Ort* reference, the Final Action fails to establish that the proposed combination of the *Hoogenboom* reference and the *Ort* reference discloses or suggests at least these limitations.

b) Claims 16-19 are Non-Obvious in View of the *Hoogenboom* and *Ort* References

As established above, the *Hoogenboom* and *Ort* references fail to disclose or suggest at least the limitations of analyzing at a first parser at least a portion of a first N data blocks after the start of a data packet to determine a data type of a subsequent data block of the data packet, wherein the subsequent data block is after the first N data blocks as recited by claim 16. Accordingly, the proposed combination of the *Hoogenboom* reference and the *Ort* reference fails to disclose or suggest each and every limitation of claim 16, and therefore also fails to disclose each and every limitation of claims 17-19 at least by virtue of their dependency from claim 26. Accordingly, the Final Action fails to establish a *prima facie* case of obviousness in support of its rejection of claims 16-19 under 35 U.S.C. § 103(a). Claims 16-19 therefore are allowable under 35 U.S.C § 103(a).

VIII. CONCLUSION

For the reasons given above, the Appellants respectfully request reconsideration and allowance of all claims and that this patent application be passed to issue.

Respectfully submitted,

30 March 2005
Date

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IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(viii))

The text of each claim involved in the appeal is as follows:

1. (Original) A system for processing transport stream data, the system comprising:

a framer module having

an input node to receive the transport stream data,

a data output node to provide a framer data which is a representation of the transport stream data, and

a data enable output node to provide a signal to indicate a valid data on the data output node;

a first parser module having

a data input node coupled to the data output of the framer module to receive the framer data,

a data enable input node coupled to data the data enable output node of the framer module;

a data output node to provide a first parser data when the framer data is a first data type, wherein the first parser data is a representation of the framer data,

a first data enable output node to provide a signal to indicate a valid first parser data on the data output node of the first parser, and

a second data enable output node to provide a signal to indicate the framer data is of a second data type.

2. (Original) The system of claim 1 further comprising:

a second parser module having

a data input node coupled to the data output node of the framer module to receive the framer data,

an enable input node coupled to the second data enable output node of the first parser module,

a data output node to provide a second parser data when the signal associated with the second data enable output node indicates the framer data is of a second data type, wherein the second parser data is a representation of the framer data;

a data enable output node to provide a signal to indicate a valid second parser data on the data output node .

3. (Withdrawn) The system of claim 2 further comprising:

a first memory controller having

a first input node coupled to the data output node of the first parser module to receive the first parser data,

and a second input node coupled to the first data enable output node of the first parser module; and

a second memory controller having

a first input node coupled to the data output node of the second parser module to receive the second parser data,

and a second input node coupled to the data enable output node of the second parser module.

4. (Withdrawn) The system of claim 3, where the first memory is a system memory, and the second memory is a video memory.

5. (Withdrawn) The system of claim 4, wherein the first parser module further includes an index output node to indicate a predefined data type, the index output node coupled to the first memory to identify a specific location within the system memory.

6. (Original) The system of claim 2, wherein the second parser module is a hardware parser.

7. (Original) The system of claim 6, wherein the second parser module has a modular layout that is substantially mutually exclusive of a modular layout of the first parser module.

8. (Original) The system of claim 6, wherein the second data type is video data.

9. (Original) The system of claim 1, wherein the data output node includes a plurality of nodes.

10. (Original) The system of claim 9, wherein the data plurality of nodes includes eight or more nodes.

11. (Withdrawn) The system of claim 1 further comprising:

a storage location to store a register set, the storage location having a first input node coupled to a status output node of the first parser module to receive status information, and a second input node coupled to a status output node of the second parser module to receive status information.

12. (Withdrawn) The system of claim 1, wherein the first input node of the storage location and the second input node of the storage location are a common input node.

13. (Original) A system for processing transport stream data, the system comprising:

a framer having a modular layout, the framer comprising

an input node to receive the transport stream data,

a data output node to provide a framer data based upon the transport stream data, and

a data enable output node to provide a signal to indicate a valid data on the data output node;

a first parser having a modular layout separate from the modular layout of the framer, the first parser comprising:

a data input node coupled to the data output node of the framer to receive the framer data,

a first data enable output node to provide a signal to indicate a first type of framer data,

a second data enable output node to provide a signal to indicate a second type of framer data.

14. (Original) The system of claim 13 further comprising:

a second parser having

a data input node coupled to the data output node of the framer to receive the framer data,

an enable input node coupled to the second data enable output node of the first parser,

a data enable output node to provide a signal to indicate the second type of framer data is to be stored.

15. (Previously Presented) The system of claim 14 further comprising:

a memory controller having

a data input node coupled to the data output node of the framer to receive the data of,

a first enable input node coupled to the data enable output node of the framer,

a second enable input coupled to the first data enable output node of the first parser,

a third enable input coupled to the data enable output node of the second parser, and

a data output to provide data to a memory.

16. (Previously Presented) A method of parsing a data packet, the method comprising:

providing a start indicator to a first parser, the start indicator indicating a first data block of the data packet, the data packet having a predetermined number of data blocks;

analyzing at the first parser at least a portion of the first N data blocks after the start of the data packet to determine a data type of a subsequent data block of the data packet, wherein the subsequent data block is after the first N data blocks;

enabling a second parser to receive the subsequent data block when the data type of the subsequent data block is a first data type; and

enabling a third parser to receive the subsequent data block when the data type of the subsequent data block is a second data type.

17. (Original) The method of claim 16 wherein the first parser is a hardware parser.

18. (Original) The method of claim 17, wherein the second parser is a hardware parser.

19. (Original) The method of claim 18, wherein the first and second hardware parsers are modular and substantially physically separate from each other.

20. (Original) The method of claim 14, wherein a data block is a byte of data.

21. (Original) The method of claim 20, wherein the predetermined number of data blocks is 188.

22. (Original) A system for storing packetized data, the system comprising:

a means for receiving a transmitted data packet;

a first parser means for analyzing a header of the data packet before a payload header is received; and

a second parser means physically separate from the first parser means for analyzing the payload header.

23. (Original) The system of claim 22, wherein the first parser further analyzes the header of the data packet before a second byte of payload header is received.

24. (Original) The system of claim 23, wherein the second parser further analyzes the payload header before a second byte of payload data is received.

25. (Withdrawn) The system of claim 22 further comprising:

a memory controller to store a first portion of payload data in video memory before storing a second portion of payload data in video memory, wherein the first portion of payload data immediately follows the payload header, and the second portion of payload data immediately follows the second portion of payload data.

26. (Withdrawn) The system of claim 25, wherein the memory controller stores the first and second portion of payload data based upon the payload header.

27. (Withdrawn) A system for storing a data stream, the system comprising:

a data processing system having

a system memory having data port, and

a video memory having a data port;

a data stream demultiplexer having

a first data port coupled to the data port of the video memory to buffer video data associated with the data stream in the video memory, and

a second data port coupled to the data port of the system memory to buffer non-video data associated with the data stream in the system memory.

28. (Withdrawn) The system of claim 27, wherein the data processing system is a general purpose computer.

29. (Withdrawn) The system of claim 27, wherein the video memory is associated with a video graphics adapter.

30. (Withdrawn) The system of claim 27, wherein the data port of the system memory is a PCI (Peripheral Communications Interface) type interface.

31. (Withdrawn) The system of claim 30, where in the data port of the video memory is an AGP (Accelerated Graphics Port) type interface.

32. (Withdrawn) The system of claim 30, where in the data port of the video memory is a PCI type interface.

33. (Previously Presented) A method of for processing transport stream data, the method comprising:

receiving a transport packet having a header and a payload, wherein the payload is associated with a primary elementary stream (PES) which can be associated with video or non-video data, wherein non-video data includes video data that is not being used;

determining if the PES is a program clock reference (PCR) PES, wherein a PCR PES is a PES that is predefined to carry a program clock reference (PCR) currently used by a decoding system; and

parsing a first set of data in the header of the transport packet using a hardware adaptation field parser when the PES is a non-video PCR PES; and parsing a second set of data in the header of the transport packet using a hardware adaptation field parser when the PES is a video PCR PES, wherein the second set includes more elements than the first set.

34. (Previously Presented) The method of claim 33, further comprising:

storing at least a portion of the PCR PES in a system memory location when the PCR PES is a non-video PES; and

storing at least a portion of the PCR PES in a video memory location when the PCR PES is a video PES.

35. (Withdrawn) A method of for processing transport stream data, the method comprising the steps of:

receiving a transport packet at a hardware transport packet parser, the transport packet having a header and a payload, wherein the payload is associated with a primary elementary stream (PES) which can be associated with video or non-video data, wherein non-video data includes video data that is not being used;

saving at least a portion of the transport packet payload in a register set when the PES is a video PES.

saving none the transport packet payload in the register set when the PES is a non-video PES.

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

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Filing Date	01/24/2000
First Named Inventor	Branko KOVACEVIC, et al.
Art Unit	2613
Examiner Name	AN, Shawn S.
Attorney Docket Number	1376-0000010
Total Number of Pages in This Submission	31

ENCLOSURES (*Check all that apply*)

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
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- [ ] CD, Number of CD(s) ____________
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (**Appeal Notice, Brief, Reply Brief**)
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	TOLER, LARSON & ABEL, LLP
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Printed name	Ryan S. Davidson
Date	30 March 2005
Reg. No.	51,596

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	[signature]
Typed or printed name	Judy Carey
Date	3/30/05

PTO/SB/17 (12-04)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/491,121
Filing Date	01/24/2000
First Named Inventor	Branko KOVACEVIC
Examiner Name	AN, Shawn S.
Art Unit	2613
Attorney Docket No.	1376-0000010

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): ______

☒ Deposit Account Deposit Account Number: 50-0441 Deposit Account Name: ATI Technologies, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
Application Type	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fee ($)**	**Small Entity Fee ($)**	**Fees Paid ($)**
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	**Fee ($)**	**Small Entity Fee ($)**
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims ______ - 20 or HP = **Extra Claims** ______ x **Fee ($)** ______ = **Fee Paid ($)** ______

HP = highest number of total claims paid for, if greater than 20

Indep. Claims ______ - 3 or HP = **Extra Claims** ______ x **Fee ($)** ______ = **Fee Paid ($)** ______

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims **Fee ($)** ______ **Fee Paid ($)** ______

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets ______ - 100 = **Extra Sheets** ______ / 50 = **Number of each additional 50 or fraction thereof** ______ (round **up** to a whole number) x **Fee ($)** ______ = **Fee Paid ($)** ______

4. OTHER FEE(S) **Fees Paid ($)**

Non-English Specification, $130 fee (no small entity discount) ______

Other: Appeal Brief 500.00

SUBMITTED BY					
Signature	[signature]	Registration No. (Attorney/Agent)	51,596	Telephone	512-327-5515
Name (Print/Type)	Ryan S. Davidson			Date	30 March 2005